What is claimed is:

1. An on-system programmable and off-system programmable chip comprising:

a control circuit;

an off-system programmable nonvolatile memory connected to said control circuit for being programmable only when connected to an external programming voltage;

an on-system programmable nonvolatile memory connected to said control circuit for being programmable under control of said control circuit;

a pumping circuit connected to said on-system programmable nonvolatile memory for supplying an internal programming voltage during programming said on-system programmable nonvolatile memory;

a volatile memory connected to said control circuit; and

an I/O unit connected to said control circuit.

2. The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises a one-time programmable memory array.

3. The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises a multi-time

programmable memory array.

4. The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises an electrically erasable programmable memory array.

5. The chip of claim 1, wherein said off-system programmable nonvolatile memory comprises a flash memory array.

6. The chip of claim 1, wherein said on-system programmable nonvolatile memory comprises an electrically erasable programmable memory array.

7. The chip of claim 1, wherein said on-system programmable nonvolatile memory comprises a flash memory array.

8. The chip of claim 1, wherein said off-system programmable nonvolatile memory and on-system programmable nonvolatile memory are spatially separated.

9. The chip of claim 1, wherein said off-system programmable nonvolatile memory and on-system programmable nonvolatile memory are selected from a memory block.

10. The chip of claim 9, further comprising a switch for

connecting said on-system programmable nonvolatile memory to said internal programming voltage.

11. The chip of claim 10, wherein said switch comprises a fuse.

12. The chip of claim 10, wherein said switch comprises a programmed circuit.

13. The chip of claim 10, wherein said switch is connected to said control circuit for determining said off-system programmable nonvolatile memory or on-system programmable nonvolatile memory to be assigned.

14. The chip of claim 1, wherein said volatile memory comprises a static random access memory.

15. The chip of claim 7, further comprising a state machine connected to said on-system programmable nonvolatile memory for preventing said on-system programmable nonvolatile memory from over erasing.

16. The chip of claim 7, wherein said flash memory array comprises a plurality of memory cells each including a flash cell connected with a MOS transistor for preventing said flash cell from

over erasing.

17. The chip of claim7, wherein said control circuit executes a state machine program for preventing said on-system programmable nonvolatile memory from over erasing.

18. The chip of claim 17, wherein said state machine program is programmed in said off-system programmable nonvolatile memory.

19. The chip of claim 17, wherein said state machine program is stored in said volatile memory.

20. The chip of claim 1, wherein said off-system programmable nonvolatile memory has a first capacity and said on-system programmable nonvolatile memory has a second capacity less than said first capacity.

21. The chip of claim 1, wherein said on-system programmable nonvolatile memory includes a plurality of programming units.

22. The chip of claim 21, wherein each of said plurality of programming units comprises a memory cell.

23. The chip of claim 21, wherein each of said plurality of programming units comprises is a bit.

24. The chip of claim 21, wherein each of said plurality of programming units comprises a byte.

25. The chip of claim 21, wherein each of said plurality of programming units comprises a word.

26. The chip of claim 6, wherein said control circuit programs a desired amendment content that is read in from said I/O unit and sent to said on-system programmable nonvolatile memory.

27. The chip of claim 7, wherein said control circuit reads a content out from said on-system programmable nonvolatile memory, stores said content to said volatile memory, amends a portion of said content to obtain an amended content, and programs said amended content to said on-system programmable nonvolatile memory.

28. The chip of claim 1, wherein said off-system programmable nonvolatile memory includes a program code for operation of said control circuit.

29. The chip of claim 1, wherein said off-system

programmable nonvolatile memory includes a control process for said control circuit to program said on-system programmable nonvolatile memory.

30. The chip of claim 1, wherein said on-system programmable nonvolatile memory is programmable under an operation mode.

31. The chip of claim 1, wherein said on-system programmable nonvolatile memory includes a data code.

32. A method for on-system programming a chip including a control circuit connected to an off-system programmable nonvolatile memory and a on-system programmable nonvolatile memory, a pumping circuit connected to said on-system programmable nonvolatile memory for providing an internal programming voltage thereto, and a volatile memory and an I/O unit both connected to said control circuit, said on-system programmable nonvolatile memory having a flash memory array, said method comprising the steps of:

Reading out a program code from said off-system programmable nonvolatile for operating said control circuit;

Reading out a content from said on-system programmable nonvolatile and storing it to said volatile memory;

amending a portion of said content for obtaining an amended content; and

programming said amended content to said on-system programmable nonvolatile memory.

33. The method of claim 32, further comprising operating a state machine for preventing said on-system programmable nonvolatile memory from over erasing.

34. The method of claim 32, further comprising executing a state machine program for preventing said on-system programmable nonvolatile memory from over erasing.

35. The method of claim 32, further comprising reading out a programming process from said off-system programmable nonvolatile memory for an operation of programming said on-system programmable nonvolatile memory.

36. The method of claim 32, further comprising switching said chip to an operation mode.

37. A method for on-system programming a chip including a control circuit connected to an off-system programmable nonvolatile memory and an on-system programmable nonvolatile memory, a pumping circuit connected to said on-system

programmable nonvolatile memory for providing an internal programming voltage thereto, and a volatile memory and an I/O unit both connected to said control circuit, said on-system programmable nonvolatile memory having an electrically erasable memory array, said method comprising the steps of:

Reading out a program code from said off-system programmable nonvolatile for operating said control circuit;

reading in a desired amendment content from said I/O unit; and

programming said desired amendment content to said on-system programmable nonvolatile memory.

38. The method of claim 37, further comprising reading out a programming process from said off-system programmable nonvolatile memory for an operation of programming said on-system programmable nonvolatile memory.

39. The method of claim 37, further comprising switching said chip to an operation mode.

40. A method for forming an on-system programmable and off-system programmable chip, comprising the steps of :

forming a control circuit in said chip;

connecting an off-system programmable nonvolatile

memory to said control circuit;

connecting an on-system programmable nonvolatile memory to said control circuit;

connecting a pumping circuit to said on-system programmable nonvolatile memory;

connecting a volatile memory to said control circuit; and

connecting an I/O unit to said control circuit;

wherein said off-system programmable nonvolatile memory is programmable by connecting with an external programming voltage from outside of said chip, and said on-system programmable nonvolatile memory is programmable by supplying an internal programming voltage from said pumping circuit.

41. The method of claim 40, further comprising programming a program code for operating said control circuit to said off-system programmable nonvolatile memory.

42. The method of claim 40, further comprising connecting a state machine to said on-system programmable nonvolatile memory for preventing said on-system programmable nonvolatile memory from over erasing.

43. The method of claim 40, further comprising programming a data code to said off-system programmable

nonvolatile memory.

44. The method of claim 40, further comprising programming a state machine program to said off-system programmable nonvolatile memory for preventing said on-system programmable nonvolatile memory from over erasing.

45. The method of claim 40, further comprising dividing a memory block into said on-system programmable nonvolatile memory and off-system programmable nonvolatile memory.

46. The method of claim 40, wherein the step of connecting a pumping circuit to said on-system programmable nonvolatile memory comprises closing a switch between said pumping circuit and on-system programmable nonvolatile memory.

47. The method of claim 40, further comprising programming a control process for said control circuit to operate said on-system programmable nonvolatile memory to said off-system programmable nonvolatile memory.

48. The method of claim 40, further comprising programming a data code to said on-system programmable nonvolatile memory.

49. The method of claim 40, further comprising programming a program code other than for operating said control circuit to said on-system programmable nonvolatile memory.